Simple Floating Immittance Simulator Using Single DVCCTA

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Abstract

This paper presents a simple floating immittance simulation circuit employing only one differential voltage current conveyor transconductance amplifier (DVCCTA) and two grounded passive components. The proposed floating simulator circuit can realize floating inductor, capacitor or resistor depending on the passive element selection. The equivalent value of the realized simulator can be tuned electronically through the transconductance parameter of the DVCCTA. The circuit also does not require any realization conditions. The proposed simulator circuit together with its applications are demonstrated using PSPICE simulation with 0.5μm MIETEC CMOS technology.

Keywords - Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA), floating simulator, inductance simulation, capacitance multiplier

1 Introduction

Floating simulator circuits are very useful active building blocks in many signal processing applications such as filter design, oscillator design and cancellation of parasitic elements. This is due to the well-known fact that the use of the physical inductor and capacitor, particularly of large values, is either not permitted or is unwanted in the integrated circuit technology. Accordingly, many circuits for the simulation of floating inductor and capacitor using various active elements have been introduced [1]-[8]. A survey of the literature shows that the floating simulator realizations in [1]-[8] still suffer from the following weaknesses: (i) they require more than one active element [1], [3]-[6], [8]; (ii) they require at least three passive components [2]-[3], [6]-[8]; (iii) they use some floating passive components [2]-[3], [7]; (iv) they cannot be tuned electronically [1]-[3], [6]-[7].

In this study, a simple realization of floating simulator using only one DVCCTA and two grounded passive components has been considered. The proposed floating simulator can be tuned electronically through the transconductance parameter of the DVCCTA. Since the circuit consists of only grounded passive components, it is suitable for integrated circuit implementation. Some applications together with simulation results are also given validating the performance of the proposed circuit idea.

2 Circuit Description

Fig.1 shows the electrical symbol of the DVCCTA. Its terminal relations can be characterized by the following equation:

\[
\begin{bmatrix}
    i_{Y1} \\
    i_{Y2} \\
    v_{X} \\
    i_{Z} \\
    i_{O+} \\
    i_{O-}
\end{bmatrix} =
\begin{bmatrix}
    0 & 0 & 0 & 0 & 0 & 0 \\
    0 & 0 & 0 & 0 & 0 & 0 \\
    1 & -1 & 0 & 0 & 0 & 0 \\
    0 & 0 & 1 & 0 & 0 & 0 \\
    0 & 0 & 0 & g_m & 0 & 0 \\
    0 & 0 & 0 & 0 & -g_m & 0
\end{bmatrix}
\begin{bmatrix}
    v_{Y1} \\
    v_{Y2} \\
    i_{X} \\
    v_{Z} \\
    v_{O+} \\
    v_{O-}
\end{bmatrix}
\]  \hspace{1cm} (1)

where \(g_m\) is the transconductance gain of the DVCCTA.

The proposed floating simulator circuit consisting of one DVCCTA and two grounded passive components is shown in Fig.2. Circuit analysis shows that the proposed floating simulator in Fig.2 has the following input impedance:

\[
Z_{in} = \frac{Z_1}{g_mZ_2}
\]  \hspace{1cm} (2)

It is clearly seen from above expression that the circuit of Fig.2 can simulate a floating inductor, capacitor and resistor depending on the selection of passive component as in the following choices:

\(Z_1\): inductor

\(Z_2\): capacitor
(i) If \( Z_1 = R_1 \) and \( Z_2 = 1/sC_2 \) are chosen, then a lossless floating inductance simulator can be obtained as:

\[
Z_m = \frac{sR_2 C_2}{g_m} = sL_{eq} \tag{3}
\]

where the realized equivalent inductance value is found to be \( L_{eq} = R_1 C_2/g_{m} \).

(ii) If \( Z_1 = 1/sC_1 \) and \( Z_2 = R_2 \) are chosen, then a lossless floating capacitance simulator can be obtained as:

\[
Z_m = \frac{1}{sR_2 C_1 g_m} = \frac{1}{sC_{eq}} \tag{4}
\]

where the realized equivalent capacitance value is equal to \( C_{eq} = R_1 C_1 g_m \).

(iii) If \( Z_1 = R_1 \) and \( Z_2 = Z_2 \) are selected, a floating resistance simulator can be realized as:

\[
Z_m = \frac{R_1}{g_m R_2} = R_{eq} \tag{5}
\]

From eqs. (3)-(5), it is obvious that the values of the \( L_{eq}, C_{eq} \) and \( R_{eq} \) can be adjusted electronically by changing the value of \( g_m \) of the DVCCTA. Moreover, by setting \( V_2 = 0 \), a grounded impedance simulator circuit can also be realized from the proposed circuit in Fig. 2.

### 3 Performance Verification

The performances of the proposed floating simulator in Fig. 2 are demonstrated by PSPICE simulation. The DVCCTA was realized by a CMOS implementation as given in Fig. 3 [9] using 0.5 \( \mu \)m MIETEC CMOS technology process parameters. The DC bias voltages were \(+V = -V = 2 \text{ V} \) and \( V_B = -1.22 \text{ V} \). The aspect ratios of the MOS transistors are listed in [9]. In this structure, the transconductance gain \( (g_m) \) can be given by [10]:

\[
g_m = \sqrt{k I_B} \tag{6}
\]

where \( k = \mu C_{ox} W/L \), \( \mu \) is the effective channel mobility, \( C_{ox} \) is the gate-oxide capacitance per unit area, \( W \) and \( L \) are channel width and length, and \( I_B \) is an external DC bias current, respectively. Thus, from equation (6), it is possible to adjust the \( g_m \) value of the DDCCTA electronically by variation of \( I_B \).

As an example for the floating inductance simulation of Fig. 2, the component values used were \( R_1 = 1 \text{ k\Omega} \), \( C_2 = 0.1 \text{ nF} \) and \( g_m \approx 0.25 \text{ mA/V} \) \((I_B \approx 100 \text{ \&\& \mu A}) \), which results in \( L_{eq} = 0.4 \text{ mH} \). The simulated voltage and current waveforms of the proposed floating inductance simulator circuit of Fig. 2 when a 1-MHz sinusoidal signal is applied are shown in Fig. 4. The impedance of the simulator versus frequency is shown in Fig. 5. It can be observed that the simulator operates correctly along the frequency range 30 kHz to 30 MHz. In Fig. 6, the frequency characteristics of the inductance simulator for various \( g_m \) values are also shown. The simulations were performed by varying \( g_m \) \( \approx 0.25 \text{ mA/V} \) \((I_B = 100 \text{ \&\& \mu A}) \), 0.35 mA/V \((I_B = 200 \text{ \&\& \mu A}) \) and 0.44 mA/V \((I_B = 300 \text{ \&\& \mu A}) \) to obtain \( L_{eq} = 0.40 \text{ mH}, 0.28 \text{ mH}, 0.22 \text{ mH} \), respectively.

![Waveforms of voltage and current for the floating inductance simulator of Fig. 2](image)

![Frequency responses of the proposed inductor](image)

![CMOS implementation of the DVCCTA](image)
Likewise, for the floating capacitance simulator of Fig.2, it is realized with the following component values : \( C_1 = 0.1 \text{ nF} \), \( R_1 = 1 \text{ k}\Omega \), and \( g_m \equiv 0.25 \text{ mA/V} \), to obtain \( C_{eq} = 25 \text{ pF} \). The time-domain signal waveforms are shown in Fig.7, which demonstrates that the circuit performs the capacitance behaviour as expected. The impedance of the simulator circuit relative to frequency is shown in Fig.8, and the plots of impedance values with different \( g_m \) are also shown in Fig.9. It appears that the simulated capacitance can be adjusted by tuning \( g_m \) of the DVCCCTA.

![Fig. 6. Magnitude responses of the proposed inductor for three different values of \( I_B \).](image)

![Fig. 7. Waveforms of voltage and current for the floating capacitance simulator of Fig.2.](image)

![Fig. 8. Frequency responses of the proposed floating capacitance simulator.](image)

![Fig. 9. Magnitude responses of the proposed floating capacitance simulator for three different values of \( I_B \).](image)

![Fig. 10. RLC bandpass filter.](image)

![Fig. 11. Ideal and simulated frequency responses of Fig.10.](image)

4 Application Examples

As an example to demonstrate an application of the proposed floating inductor of Fig.2, it is employed in the RLC bandpass filter as shown in Fig.10. The floating inductor circuit is simulated with the following component values : \( R_1 = 1 \text{ k}\Omega \), \( C_2 = 0.1 \text{ nF} \), and \( g_m \equiv 0.25 \text{ mA/V} \) \( (I_B = 100 \text{ \mu A}) \), which results in \( L_{eq} = 0.4 \text{ mH} \). Fig.11 shows the frequency responses of the bandpass filter of Fig.10, which appears that the ideal and simulated magnitude and phase responses are in good agreement for a set of selected values over several decades.

Furthermore, to verify the performance of the derived capacitance simulator of Fig.2, the resistively terminated LC highpass shown in Fig.12 filter was designed and simulated. This filter was designed to realize third-order highpass Butterworth characteristic with the de-normalized cut-off frequency of \( f_c = a_3/2\pi = 3.18 \text{ MHz} \). The circuit was simulated with the ideal capacitor and our proposed floating capacitor. For this purpose, the following component values were taken for the floating capacitance simulators in Fig.2 : \( C_1 = 0.1 \text{ nF} \), \( R_2 = 1 \text{ k}\Omega \), and \( g_m \equiv 0.25 \text{ mA/V} \). The theoretical and simulation results for the filter of Fig.12 are given in Fig.13.

\[
\begin{align*}
V_{in} & \xrightarrow{L_{eq}} C = 1 \text{ nF} \\
\xrightarrow{R = 1 \text{ k}\Omega} & V_o
\end{align*}
\]
\[ R_L = 1 \, \text{k}\Omega \]

\[ C_{eq} = 25 \, \text{pF} \]

\[ L = 50 \, \mu\text{H} \]

\[ C_{eq} = 25 \, \text{pF} \]

\[ R_S = 1 \, \text{k}\Omega \]

**Fig. 12.** Third-order Butterworth highpass filter.

**Fig. 13.** Theory and simulated magnitude responses of Fig.12.

### 5 Conclusion

In this article, the floating simulator circuit using a single DVCCTA and two grounded passive components is presented. The values of the simulated inductance, capacitance and resistance can be controlled electronically by the \( g_{m} \)-value of the DVCCTA. PSPICE simulation results with 0.5-μm MIETEC CMOS technology verify the workability performance of the proposed floating simulator circuit. The operation of the proposed circuit is validated on the second-order bandpass and third-order Butterworth highpass filters.

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### References


