Design of High-Order Phase-Lock loops Controller using Simulink

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1 Introduction

Phase-Locked Loops (PLLs) have developed into many other electrical, instrument control and electronic systems. Inattentive of their individual implementation, with their related specific problems, the basic theory common to all PLLs is not easy to understanding. Fundamentally, this is because it is feedback system and exhibits an intrinsic nonlinear nature. Even assuming approximate linear model, analysis and subsequent design, of any higher-order(above two) PLL is challenging. To make things even more difficult, the literature on PLLs is plagued with some misconceptions which have perpetuated for years. Among these misconceptions are the use of parameters to characterise the PLL which are meaningless for higher-order PLLs, such as the loop filter (LF) classifications (passive as opposed to active) that do not make sense today in implementations dominated by charge pump (CP) topologies, and the confusion of order and type [1]. The accurate analysis of third-order phase-locked loops (PLLs) , those including a second-order loop filter (LF) , is normally eluded because it is very complex.

The goal of this paper however, is to propose an alternative approach to the intuitive and analytic design of third -, and even fourth-order loops, as a natural extension of second-order PLL. The approach will also be seen as related to the extension of a conventional PLL (second order) with the so called "aided acquisition" loops [2]. The concepts shown here are general , but of particular interest in applications where the PLL need to operated in a wide hold range, i.e., not a small fraction of the free running frequency (FRF) of the oscillator.

The design and constructional features of the whole system are presented in this paper. Experimental work has been carried out on the induction heating system to measure the operation performance under various loading conditions. Experimental results indicate that the operates successfully with a power factor very closed to unity. A simulation model has been develop using Simulink , which has been used to analyse and design the PLL control system. A mathematical model of the system has also been developed in discrete time, with which the stability of the system can be assessed.

2 Experimental setup

Block diagram and induction heating circuit is shown in Fig.1 and Fig.2, where it may be seen that the output power is controlled by a single phase controlled rectifier and that the inverter is of the voltage-fed load resonant type. A high-frequency impedance matching transformer with a turns ratio 33/6 has been designed and constructed with nearly condition is nature, and this is complex match the impedances of the converter and induction heating coil.

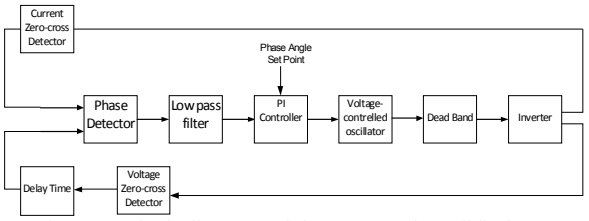

Figure1. Block diagram of the proposed modified PLL

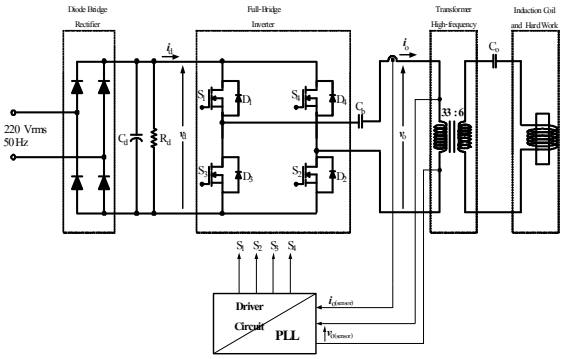

Figure 2. High frequency Induction heating circuit

2.1 Second-order PLL and Aided Acquisition loops

A typical model of an analog PLL including a phase detector (PD), an LF, and a voltage-controlled oscillator (VCO) shown in Fig.3. Signals θ_{in} and θ_{out} are input and output phases.VCO is usually modelled by integrator, since phase is the integral of instantaneous frequency with gain K_v rads/(V.s). As for the PD, its model depends on the implementation, but it is usually approximated by the phase difference with in limited range, scaled by a gain K_θ. The LF is assumed linear, and thus the simplest case, apart from trivial PLL with no filter, is a first-order one. Thus, its most general transfer function, assuming unity dc gain, is

$$H_{LF}(s) = H_1(s) = (1+\frac{s}{\omega_{1z}}) \Big/ (1+\frac{s}{\omega_{1p}}) \qquad (1)$$

equation for this particular case can be found elsewhere, although they are quite often buried by particular electrical parameters dependent on the implementations of the filters. Since dc filter gain is unity, PLL gain is defined as $K=K_v.K_\theta$.

2.2 Third-order PLLS and Higher-order PLLs

This latter model, though conceptually interesting, can be further simplified if one takes into consideration that the VCO can be modelled as an integrator. Then , integration by the VCO and the differentiator operation, comprising the scaling factor, cancel out giving the equivalent scheme shown in Fig.5

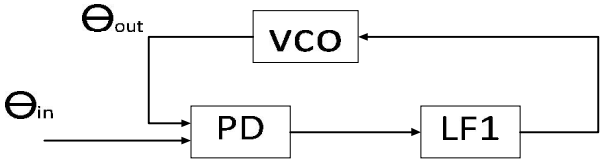

Figure 3. PLL block diagram

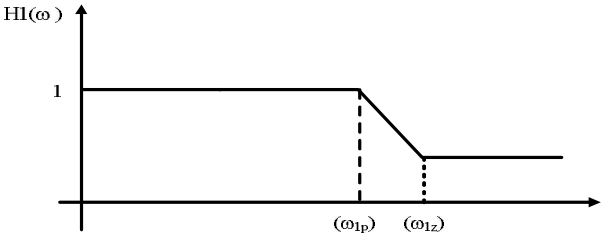

Figure 4. First-order loop-filter frequency response

Clearly, LF2 can be now combined with LF1 to give a single LF. If LF1 is of order one, as in (1), and LF2 is also of order one with a single pole at ω_2

$$H_2(s) = 1 \Big/ (1+\frac{s}{\omega_2}) \qquad (2)$$

We come up with a second-order LF and thus a third-order PLL. The gobal response of such filter, also known as Przedpelski Filter [5], is shown below, and its Bode plot present in Fig.6.

$$H_{LF}(s) = H_1(s)\frac{1}{1-H_2(s)} = \frac{\omega_2}{s}\frac{(1+\frac{s}{\omega_{1z}})(1+\frac{s}{\omega_2})}{1+\frac{s}{\omega_{1p}}} \qquad (3)$$

In this process we have gained some insight into meaning of each one of the time constants and signals into the circuit. A constant value is an indication of the situation described. Such a difference signal can be used the appropriate delay to further correct the VCO input and minimize the phase error. The proposed modification is shown in the Fig.7.

If the filter LF3 is of first-order too, with cut-off frequency ω_3, then, the overall performance of the two loops can be assimilated to a single LF whose response is now.

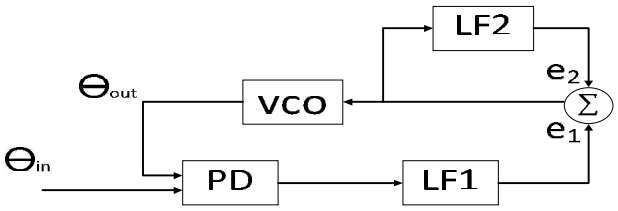

Figure 5. Second-order PLL block diagram

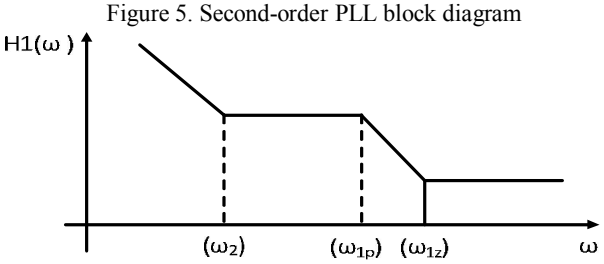

Figure 6. Second-order loop-filter frequency response

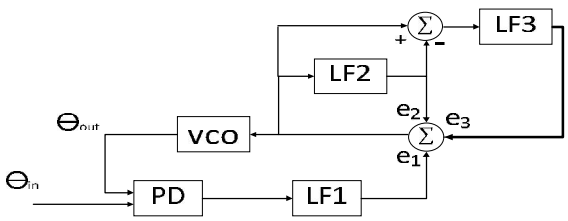

Figure 7. Third-order PLL block diagram

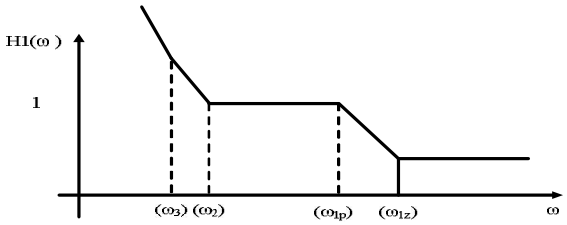

Figure 8. Third-order loop-filter frequency response

$$H_{LF}(s) = H_1(s)\frac{1}{(1-H_2(s))(1-H_3(s))}$$

$$= \frac{\omega_2.\omega_3}{s^2}\frac{(1+\frac{s}{\omega_{1z}})(1+\frac{s}{\omega_2})(1+\frac{s}{\omega_3})}{(1+\frac{s}{\omega_{1p}})} \qquad (4)$$

Its bode plot is represent in Fig.8 where the time constant of the new filter, $1/\omega_3$, is higher than $1/\omega_2$. This condition is however not need for the correct operation of loop since, according to (4), the two poles can be exchange.

3 Simulation Model

A Simulink model, which allows an evaluation of how the various feedback loop affect the operation of the PLL, and the evolution of the signals involved, was implemented, We will proceed by analyzing, first the operation of second-order loop and then appraise how it is affected by the introduction of the new loops. This will mimic the design procedure to be followed , regardless of whether the LF is implemented in a compact manner in the final design(just plug-in the LF parameters from design), or with the explicit feedback loop

4 Conclusion

We have present high-order PLLs, as a natural extension of type I PLLs of lower order (one, two and even three). Although this approach in general ,we have restricted ourselves to showing practical situation with order no higher than five, and type no higher than III. The theorectical frame work is based on the PLL model, and in particular the LF, through serval feedback loop.

The analysis and the results presented in this paper support two basic assumptionsthat, although not original, are not generally and explicitly accepted in the literature. First, there is the assumption that PLL gain, K, characterises PLL bandwidth more than any otherparameter. This is particularly true if we start the design with a highly damped, type I, PLL. Secondly, Type, much more than order, describes OLL performance.

References

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